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☐	L45	l31 and L40	37
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☐	L39	710/8.ccls.	121
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☐	L35	l32 same string	4
☐	L34	(processor near3 (id or identity or identif$9)) same string	67
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☐	L28	((processor or microprocessor) near3 maximum near3 (speed or frequency))	106
☐	L27	L26 same output$4	1
☐	L26	(retriev$4 near3 maximum near3 (speed or frequency))	18
☐	L25	l4 same (detect$4 or sens$4)	0
☐	L24	l4 with (detect$4 or sens$4)	0
☐	L23	l7.clm.	0
☐	L22	l7.ab.	0
☐	L21	US-20030097602-A1.did.	1
☐	L20	US-20030097602-A1.did.	1
	DB=USPT,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR		
☐	L19	l2 same verif$9	1
☐	L18	l15.ab.	10
☐	L17	L14.ab.	237

☐	L16	L14 with ((plurality or multiple) near3(processor or microprocessor))	1
☐	L15	L14 with (processor or microprocessor)	53
☐	L14	(version near5 match$4)	1427
☐	L13	L4 and (interpret$7 near5 string)	1
☐	L12	L6 and interpret$7	17
☐	L11	L4 and interpret$7	88
☐	L10	L4 same interpret$7	0
☐	L9	L4 same interpret$4	0
☐	L8	L7 same interpret$4	0
☐	L7	L4 with (processor or microprocessor or computer)	42
☐	L6	L4 same (processor or microprocessor or computer)	100
☐	L5	L4 same identif$9	10
☐	L4	(maximum adj operating adj frequency)	1220
☐	L3	L2 same (processor or microprocessor or computer)	2
☐	L2	(identif$9 or identity or indicat$4 or determin$4 or calculat$4) near3 (maximum or highest or fastest) near3 frequency near3 operat$4	54
☐	L1	(brand adj string)	4

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L46: Entry 2 of 3 File: PGPB May 8, 2003

DOCUMENT-IDENTIFIER: US 20030088782 A1
TITLE: Biometrics template

Detail Description Paragraph:
[0043] When a user wishes to access the network, they present their eye 12 to the biometrics scanning station 30, while also presenting a smart card 38 having that user's identification code 22 stored thereon to the smart card reader 32. The scanning station 30 converts features of the user's eye 12 to a biometrics identifier, which is passed to the processor 36 together with the identification code 22. The processor then determines from the look-up table the location on the network of a suitable number of identification strings 24 having that identification code 22, sufficient to reconstruct the key 16. A request is sent to the appropriate terminals 26a, 26b, 26c for the relevant identification string 24, which strings 24 are then returned to the processor 36.

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L35: Entry 2 of 4 File: PGPB Sep 25, 2003

DOCUMENT-IDENTIFIER: US 20030182545 A1
TITLE: METHOD AND APPARATUS FOR IMPLEMENTING A REGISTER SCAN PROCESS

Detail Description Paragraph:
[0019] P0 directory 260 contains the identifier `P0`, a pointer to a peer d-node for P1 directory 270, and a pointer to an entry for processor ID entry 265. Processor ID entry 265 contains a type indicating what type of entry is stored (a string in this instance), a value which holds the value of the entry (`PIII001` in this instance), an ID indicating the identification of the entry (`Processor ID` in this instance) and a pointer to another entry for processor speed entry 268. Processor speed entry 268 contains a type indicating what type of entry is stored (a string in this instance), a value which holds the value of the entry (`Auto` in this instance), an ID indicating the identification of the entry (`Processor Speed` in this instance), and a pointer to another entry which is not shown.

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L29: Entry 1 of 2 File: PGPB Mar 11, 2004

DOCUMENT-IDENTIFIER: US 20040049709 A1
TITLE: Method and apparatus for limiting processor clock frequency

Abstract Paragraph:
A method and apparatus for limiting a processor clock frequency includes an overclocking prevention circuit. The overclocking prevention circuit includes a frequency limiting circuit having programmable fusible elements. The frequency limiting circuit outputs a signal identifying a maximum processor clock frequency based on the state of each of the fusible elements. A comparator circuit compares a selected processor clock frequency to the maximum processor clock frequency to determine if the selected processor clock frequency is permitted. If the selected processor clock frequency is not permitted, then the processor is not allowed to operate at the selected clock frequency.

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L30: Entry 13 of 13 File: PGPB May 16, 2002

DOCUMENT-IDENTIFIER: US 20020059537 A1
TITLE: Method and apparatus for limiting processor clock frequency

CLAIMS:

1. An apparatus for limiting a processor clock frequency comprising: a frequency limiting circuit including one or more programmable fusible elements, the frequency limiting circuit outputting a signal identifying a maximum processor clock frequency based on the state of each of the fusible elements; a comparator circuit coupled to the frequency limiting circuit, said comparator circuit receiving a signal identifying a selected processor clock frequency as a first input and receiving the signal identifying the maximum processor clock frequency as a second input, said comparator circuit outputting a signal indicating whether or not the selected processor clock frequency is greater than the maximum clock frequency.

4. The apparatus of claim 1 and further comprising a memory location for storing information indicating whether or not the selected processor clock frequency is greater than the maximum processor clock frequency.

6. A frequency limiting circuit comprising: a plurality of fusible elements which can be programmed to select a maximum processor clock frequency; frequency limiting selection logic coupled to the fusible elements, said selection logic receiving a multi-bit input signal identifying a selected maximum processor clock frequency, said selection logic outputting a signal identifying a maximum processor clock frequency based on the programmed state of each fusible element and the received multi-bit input signal.

7. The frequency limiting circuit of claim 6 wherein said frequency limiting selection logic outputs a signal identifying a maximum processor speed as a logical ORing of the programmed state of each fusible element and the received multi-bit input signal.

8. An apparatus for limiting a processor clock frequency comprising: an external circuit, said external circuit outputting signals identifying a selected processor clock frequency; a processor coupled to the external circuit and receiving the signals identifying the selected processor clock speed; said processor comprising: an overclocking prevention circuit, said overclocking prevention circuit including a plurality of programmable fusible elements that are programmed to identify a maximum processor clock frequency, and a comparator for comparing the programmed maximum processor clock frequency to the selected processor clock frequency, said overclocking prevention circuit preventing operation of the processor at the selected processor clock frequency if the selected processor clock frequency is greater than the programmed maximum processor clock frequency.

12. A method of limiting processor clock frequency comprising the steps of: programming one or more fusible element to set a maximum processor clock frequency; receiving a signal selecting a processor clock frequency; comparing the selected processor clock frequency to the maximum processor clock frequency; and preventing

operation of the processor at the selected processor clock frequency if the selected processor clock frequency is greater than the maximum processor clock frequency.

13. The method of claim 12 wherein said step of preventing comprises the step of halting the processor if the selected processor clock frequency is greater than the maximum processor clock frequency.

14. The method of claim 11 wherein said step of preventing comprises the step of automatically operating the processor at a clock frequency that is less than or equal to the maximum clock frequency if the selected processor clock frequency is greater than the maximum processor clock frequency.

15. A method of setting a maximum processor clock frequency comprising the steps of: programming a first of a plurality of programmable fusible elements to set a first maximum processor clock frequency; programming one or more additional fusible elements to set a lower maximum clock frequency, wherein the programming of each said additional fusible element can only set a maximum clock frequency that is successively lower.

16. A method of setting a maximum processor clock frequency comprising the steps of: setting a first maximum processor clock frequency by programming fusible elements and/or setting bits of a multi-bit input signal; and adjusting the first maximum processor clock frequency to a lower clock frequency by programming one or more additional fusible elements or by setting additional bits of the multi-bit input signal.

L5: Entry 7 of 10 File: USPT Jun 13, 1989

DOCUMENT-IDENTIFIER: US 4839834 A
TITLE: Speed detecting apparatus

Detailed Description Text (3):
Referring to FIG. 1, an encoder 1 mechanically coupled to an electric motor (not shown) generates sine-wave signals A and B, having a phase difference of 90.degree. therebetween, when it rotates by an amount corresponding to 1/m (m: a large integer) of one complete encoder revolution. The output signals A and B of the encoder 1 are applied to comparators 2 and 3 where the signals A and B are compared with zero volts and are converted into squarewave signals AS and BS respectively. It will be seen in FIGS. 2 and 3 that the positive half wave of the signals A and B corresponds to the "1" level of the signals AS and BS. The sine-wave signal A is applied also to an A/D converter 4. The square-wave signal AS is applied to a pulse forming circuit 5. In synchronism with the leading edge and trailing edge of the waveform of the square-wave signal AS, the pulse forming circuit 5 generates zero-crossing pulses AP. This zero-crossing pulse signal AP is applied to a reversible counter 7 through a normal-reverse change-over circuit 6. In response to a direction decision signal RD applied from a direction decision circuit 11, described later, the normal-reverse change-over circuit 6 changes over the polarity of the zero-crossing pulse signal AP. More precisely, the count of the reversible counter 7 is incremented when the encoder 1 rotates in the normal direction, but the count of the reversible counter 7 is decremented when the encoder 1 rotates in the reverse direction. The zero-crossing pulse signal AP is applied also to a set terminal SET of a register 8. As soon as a pulse of the zero-crossing pulse signal AP is applied to the set terminal SET of the register 8, the count of a clock counter 9 is transferred to and registered in the register 8. A clock pulse generator 10 generates clock pulses at a predetermined frequency, and the clock counter 9 counts these clock pulses. The frequency of the clock pulses generated from the clock pulse generator 10 is selected to be higher, by one decimal place or more, than the maximum operating frequency of the encoder 1. In the meantime, the square-wave signals AS and BS are applied to a direction decision circuit 11 and a quadrant decision circuit 12. The operation of the direction decision circuit 11, which discriminates the direction of rotation of the encoder 1, is such that it decides that the encoder 1 is rotating in the normal direction when the phase of the square-wave signal AS lags that of the square-wave signal BS, but it decides that the encoder 1 is rotating in the reverse direction when the phase of the square-wave signal AS leads that of the square-wave signal BS. The phase relationship between the square-wave signals AS and BS can be identified, for example, by reference to the level of the square-wave signal BS at the rise time of the square-wave signal AS. Depending on the relative levels of the square-wave signals AS and BS, the quadrant decision circuit 12 decides the quadrant (0-.pi./2, .pi./2-.pi., .pi.-3.pi./2, 3.pi./2-2.pi.) of the square-wave signal As and generates a 2-bit quadrant decision signal D. That is, the 2-bit quadrant decision output signal D of the quadrant decision circuit 12 represents 0 (the first quadrant) when both the square-wave signals AS and BS are in their "1" level; 1 (the second quadrant) when the square-wave signal AS only is in its "1" level; 2 (the third quadrant) when both the square-wave signals AS and BS are in their "0" level; and 3 (the fourth quadrant) when the square-wave signal BS only is in its "1" level. This 2-bit quadrant decision signal D is used to select a corresponding area of a memory 13 which stores a table of values of four kinds of inverse sine

L5: Entry 1 of 10 File: USPT Apr 13, 2004

DOCUMENT-IDENTIFIER: US 6720643 B1
TITLE: Stacked semiconductor module

Detailed Description Text (14):
Identification (step 404) of the IC dies preferably comprises firstly ascertaining (step 408) which integrated circuit dies are functioning. This may be done by testing each of the IC dies within the stacked semiconductor module. The determination of which IC dies are functional may include a large number of tests of the functionality of each IC die. These tests may include tests performed on each IC die prior to assembly of the semiconductor module, and may include tests that ensure each IC die operates properly at a specified minimum or threshold operating frequency, that a memory array in each IC die operates properly at a specified minimum or threshold core timing grade, as well as at specified minimum and maximum supply voltages. In the preferred embodiment, during the testing of the IC dies in the semiconductor module, a maximum operational frequency is ascertained (step 410) for each functional IC die in the semiconductor module by testing the operation of each IC die at a range of operating frequencies. The lowest of the maximum operating frequencies of the functional IC dies is selected as the maximum operating frequency of the semiconductor module. Thus, the maximum operating frequency of the semiconductor module is a frequency at which it is known that all the functional IC die in the module can properly operate.

Detailed Description Text (16):
The programmable memory device is then programmed (step 406) to identify the selected functional IC dies having the desired characteristics. The programmable memory device may also be programmed to indicate the maximum operating frequency of the semiconductor module, the maximum core timing grade of the semiconductor module, as well as other characteristics of the semiconductor module or its functional IC dies that may be of use to a controller used in conjunction with the semiconductor module. The information stored in the programmable memory device enables the controller to separately address the functional IC dies in the semiconductor module.

L5: Entry 2 of 10 File: USPT Mar 2, 2004

DOCUMENT-IDENTIFIER: US 6700390 B2
TITLE: Adjustment and calibration system to store resistance settings to control chip/package resonance

Detailed Description Text (14):
The host interface (not shown) may be used to operatively connect to a separate computer system. For example, a tester (550) communicates with the test processor unit (552). The tester (550) instructs the test processor unit (552) to adjust the digital potentiometer (554). The tester (550) measures the maximum operating frequency of the CPU. The CPU maximum operating frequency may be used as a representation of the chip/package impedance. The tester (550) may use the CPU maximum operating frequency to determine the effect of the adjustment. A variety of different adjustments may be made in an effort to identify the adjustment settings that produce the CPU maximum operating frequency. For example, the tester (550) may be used to adjust the digital potentiometer (554) to modify the chip/package impedance. The digital potentiometer (554) may be adjusted until the CPU maximum operating frequency is obtained.

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L13: Entry 1 of 1 File: USPT Feb 11, 2003

DOCUMENT-IDENTIFIER: US 6518754 B1

**** See image for Certificate of Correction ****

TITLE: Powerful bonded nonconducting permanent magnet for downhole use

Brief Summary Text (14):

Two features limit the effectiveness of the Taicher '479 device. First, the grains of Samarium-Cobalt must satisfy a size constraint dictated by the operating frequency of the tool. The particle diameter must be less than the skin depth of the radio frequency (RF) at the maximum operating frequency. Secondly, the magnet in the Taicher '479 device must be segmented into electrically isolated blocks. This requirement arises from the fact that the epoxy resin-bonded Samarium-Cobalt material has a significant residual conductivity.

Detailed Description Text (2):

FIG. 1 shows a well logging apparatus (referred to as a "tool string" 22) disposed in a wellbore 11 drilled through earth formations 21, 23, 25, 27. The tool string 22 includes various sensors for measuring selected properties of the earth formations 21, 23, 25, 27 particularly within a predetermined volume of investigation 58, also referred to as the "sensitive volume". The tool string 22, which can include a nuclear magnetic resonance ("NMR") apparatus according to the invention, is typically lowered into the wellbore 11 by means of a winch-driven armored electrical cable 30 or similar conveyance known in the art. The NMR apparatus can be included in an NMR probe 42, comprising an antenna (not shown in FIG. 1), and a permanent magnet assembly (not shown separately in FIG. 1) made according to the invention forming part of the tool string 22. The tool string 22 can be connected, through the electrical cable 30, to surface equipment 54 including circuitry (not shown separately) for decoding and interpreting signals sent over the cable 30 from the tool string 22. Circuits for decoding and interpreting the signals sent by the tool string 22 over the cable 30 are well known in the art.